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Self-Triggered SCR in Output Driver for Enhanced ESD Robustness

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***Abstract*—This paper presents an enhanced ESD (Electrostatic Discharge) protection solution for output drivers without additional protection devices. The output drivers in low and high voltage CMOS technologies are often susceptible against the ESD stresses with and without the ESD protection devices. The proposed structure shows significantly improved ESD immunity using a consolidated NPBL (N Plus Buried Layer) mask underneath an ESD protection SCR (Silicon Controlled Rectifier) for the VCC to the ground and the output drivers, which are effectively triggered when ESD events occur. This consolidated NPBL plays an important role of a booster for faster triggering than other parasitic devices.**

I. INTRODUCTION

One of the ESD protection devices utilized for high voltage CMOS technologies is the SCR, but its triggering voltage is generally quite high and can vary between 40 and 100V depending on the process and design [1, 2]. When positive ESD events occur in output respect to Ground utilizing a conventional ESD protection scheme, the ESD current's path is expected to travel to ground via a forward diode of the MPPWR (Medium voltage P-type Power device) and an SCR as shown Fig 1. However, the MNPWR (Medium voltage N-type Power device) typically turns on earlier than the SCR because its breakdown voltage is lower than that of the SCR. The MNPWR is very susceptible to ESD stresses because of its very low dose junction between the drain and source thereby creating hot spots due to excessive heating. Another possible discharge path for an ESD event on an output pin is via the parasitic PNP (Q3 on Fig 2), but this also proves ineffective and does not turn on due to the higher trigger voltage between the NPBL (Base) and the Substrate (Collector) as compared to the that of the MNPWR device. This is the primary reason that the output pin tends to have compromised ESD performance when utilizing the conventional ESD protection scheme for an output driver. One way to approach this is for the trigger voltage of the parasitic PNP to be lowered by laying out the MPPWR, MNPWR (Medium voltage N-type Power device) and the SCR on the same NPBL. The parasitic PNP on the consolidated NPBL is subsequently turned on at a lower voltage and triggers the SCR simultaneously. As a result, the triggered SCR will have an improved capability for clamping ESD. This paper provides details of a novel concept and methodology to improve the ESD performance of an ESD sensitive output pin.

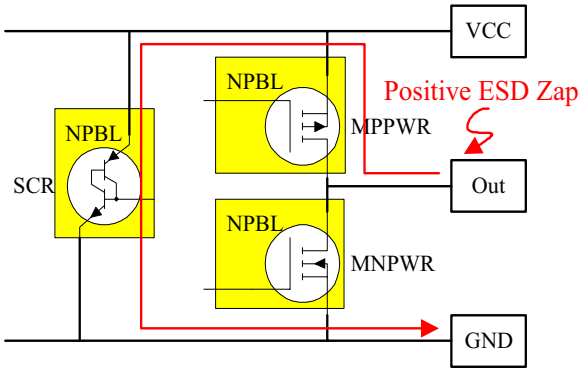

Fig.1 An ideal ESD current path in a conventional output driver [Individual NPBL (Yellow box) formed at the output driver].

II. SCHEMATIC AND DEVICE BEHAVIOR

This section presents a conventional ESD scheme (A) as well as a new concept (B). A triggering voltage for the conventional ESD scheme is depending on breakdown voltage of each device in the conventional output driver that caused low ESD threshold because undesired current paths are established and should not handle such a high current in the output driver during ESD events. A consolidated NPBL in the proposed scheme, however, helps turning on ESD protection device effectively and improves ESD immunity.

A. Individual NPBL Output Driver

Fig 2 shows a cross section view of an ideal ESD current path in a conventional output driver, as initially depicted in Fig 1. The cross section view illustrates major parasitic devices and the current path for the output driver as well as an SCR. The ESD current paths are established through the Q5 when ESD events occur with output respect to ground. In this specific scheme, the SCR ESD protection device is not triggered. It means that the MNPWR output device needs to endure and absorb ESD current fully by itself when positive ESD events occur between the output and the ground. The ESD protection SCR device from the VCC to the ground occupies area without any meaning and it needs additional ESD protection for the VCC pin. Most of the ESD current will flow into the Q5 because the breakdown voltage of the Q5 is lower than the Q3. This in turn results in lowered ESD immunity because the MNPWR has current crowding when a high and fast edge rate ESD current is applied to the output.

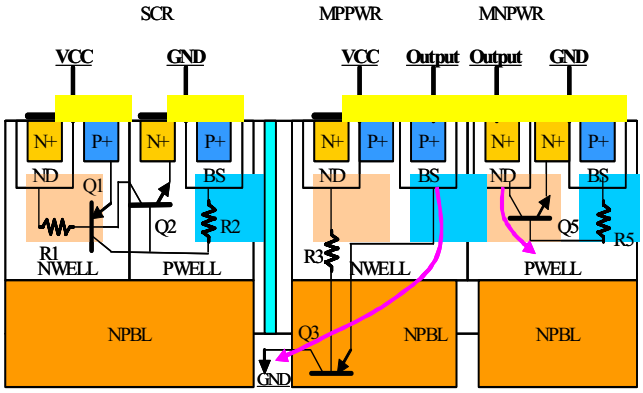

Fig.2 Cross section view of a conventional output driver.

TLP (Transmission Line Pulse) testing, as demonstrated in Fig 3, illustrates how the MNPWR works during an ESD event for a conventional output driver. The MNPWR can not endure 1.4A (which is the theoretical equivalent current of a device HBM (Human Body Model) threshold of 2KV) even though the total width of the MNPWR is over 2000um because excessive electric field in the Drain region can affect its junction due to current crowding. In order to endure ESD current by the MNPWR itself without ESD protection devices, it has to be reduced the electric field especially, in the Drain. One of the methods to reduce the field is characterization of DCGS (Drain Contact to Gate Space) of MNPWR. However, there is a tradeoff between device's performance such as on-resistance, capacitance, etc. and ESD immunity. When the MNPWR is damaged, the leakage current in the device is significantly increased and shows very stiff on- resistance because the Drain and the Source junctions have been damaged during the ESD events, as depicted in Fig 5.

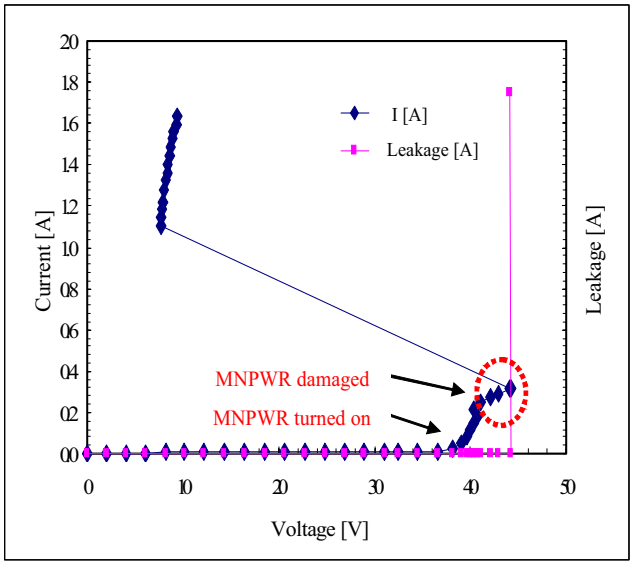

Fig.3 TLP characteristics on a conventional output driver.

Fig 4 indicates a hot spot after applying a 2KV HBM zap to a bare die and then tested at wafer level. An H.E.A (Hot Electron Analyzer) was used in order to see any abnormal current path created by the ESD induced event. The HEA results reflected similar findings achieved through TLP which indicate current crowding along the stripes of the MNPWR.

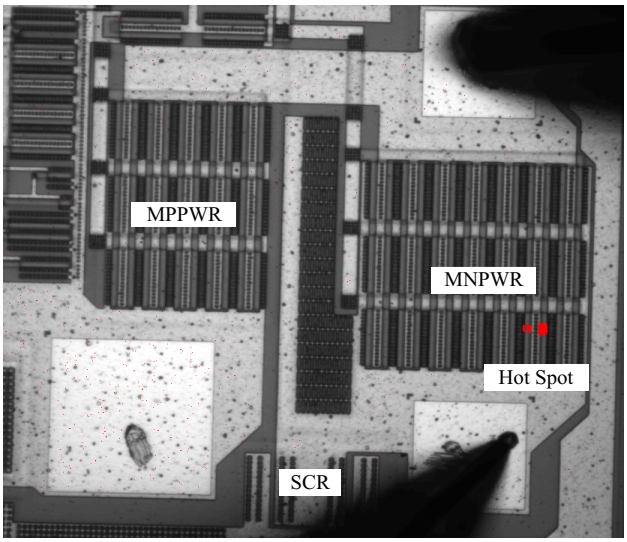

Fig.4 HEA(Hot Electron Analyzer) shows hot spot after positive 2KV HBM zapped.

FA (Failure Analysis) was then performed on the 2KV HBM zapped device to isolate and identify the location and extent of damage. Top layers were removed so that the junction damage between the Drain and the Source of the MNPWR could be observed. Consequently, the output driver with individual NPBL islands among MPPWR, MNPWR, and

SCR utilized in this technology was demonstrated to not guarantee sufficient ESD immunity. In order to prevent the MNPWR damage, a new ESD protection scheme in the output driver needed to be developed.

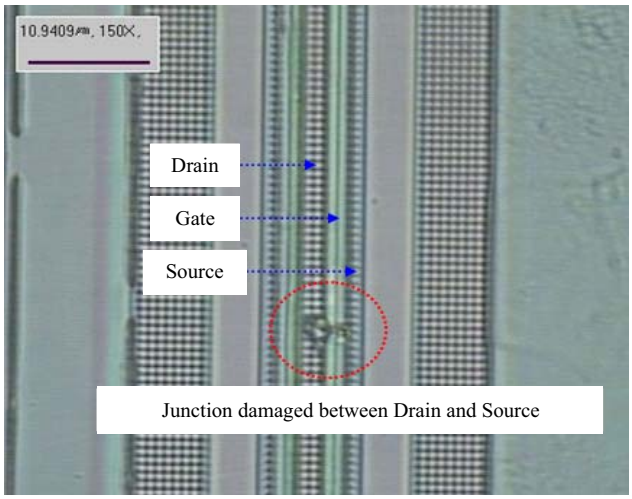

Fig.5 Damaged site on MNPWR after positive 2KV HBM zapped.

B. Consolidated NPBL Output Driver

A new concept of the output driver was then developed which merges a single NPBL with an MPPWR, MNPWR and SCR as shown in Fig 6. This creates the self-triggered SCR. If the NPBL is merged with the output driver, then a parasitic PNP (Q4) supplies base current to Q2 and becomes a triggering source of the designed SCR which is composed of the Q4 and the Q2 like an MLSCR [3]. This approach results in an effective loop to turn on the SCR at the appropriate time while not allowing the flow of ESD current to the MNPWR. This then protects the MNPWR during ESD events, such as positive HBM zaps applied to the output versus ground as demonstrated by the TLP characteristics depicted in Fig 7.

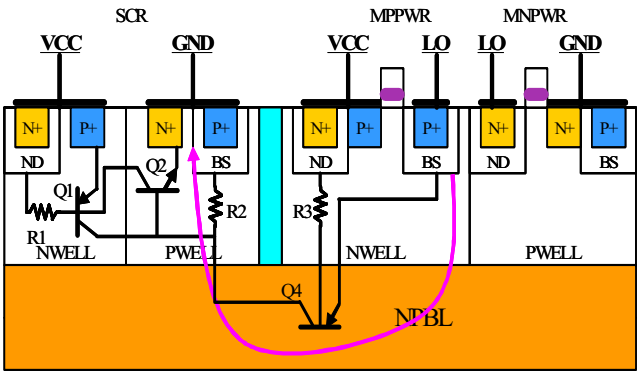

Fig.6 Cross section of consolidated NPBL output driver

The TLP characteristics in Fig 7 also depict the SCR and a series forward diode of the MPPWR during turn on. If the SCR is triggered by the Q4 as shown in Fig 6 then the It2 will exhibit more than 2.5amps, which is roughly equivalent to an HBM of 3.5KV. The formula used for calculating the overall HBM sensitivity is V_{HBM} = It2 x R_{HBM} x M. where, M is the correlation factor.

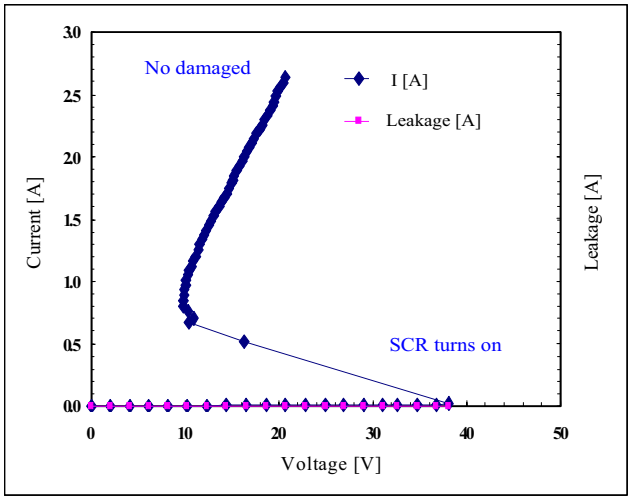

Fig.7 TLP characteristics of Fig.6

As shown in Table 1, the triggering voltage was the same for MNPWR as well as the MPPWR, but the SCR has a much higher triggering voltage than just the output power devices and the MNPWR alone which endured just 500V HBM. By contrast, a merged single NPBL output driver survived up to 3.5KV HBM because the ESD current path was effectively rerouted and the SCR device could then absorb significant ESD current, especially when exposed to positive ESD events that may have occurred. If negative ESD events occur with an output respect to ground scenario, then a forward diode of the MNPWR turns on, also insuring adequate protection. By contrast to HBM which is traditionally an area where ESD protection is difficult to achieve in such a scenario, the CDM (Charged Device Model) threshold was found to be 2KV in an 8 lead SOP (Small Outline Package) for both the conventional output driver as well as the proposed one. No change was noted in CDM between the conventional and proposed solutions, which are theorized to be due in part to the overall package capacitance rather than the protection structures utilized by the output drivers.

TABLE 1 THRESHOLDS FOR DISCRETE DEVICES OF AN OUTPUT DRIVER AS WELL AS PROTECTION DEVICES TESTED AT WAFER LEVEL.

	Individual NPBL output driver	
	Trigger Voltage	***HBM threshold***
SCR	56V	8000V
MNPWR	39V	500V
MPPWR	39V	1500V

TABLE 2 STANDARD ESD TEST RESULTS ON THE PACKAGE .

	Individual NPBL output driver		Consolidated NPBL output driver	
	JESD22-A114	*JESD22-C101*	*JESD22-A114*	*JESD22-C101*
8 LD SOP	**500V**	**2000V**	**3500V**	**2000V**

III. CONCLUSION

In order to protect a medium voltage output driver exposed to ESD events, a merged NPBL layer has to be formed in the output driver along with an ESD protection device. Fig 8 shows an equivalent circuit for an individual NPBL layer and Fig 9 shows a merged NPBL layer. The goal is to route the ESD current path through a forward diode of the MPPWR in series with the SCR to protect the MNPWR of the output driver. By doing so, the MNPWR current path is ignored when the output is exposed to a described ESD current path in an equivalent schematic, as depicted in Fig 9.

Fig 8 shows an individual NPBL output driver with no triggering path for the SCR ESD protection device. In this specific case, the triggering voltage of a parasitic PNP (Q3) in the MPPWR is much lower than the SCR. It will essentially never turn on when subjected to ESD events. However, Fig 9 illustrates a merged NPBL for the output driver as well as the SCR that can be triggered by a parasitic PNP (Q4) and provides an ESD current path, effectively eliminating the chance of ESD damage on the output driver. With this scenario, the Q4 triggers the NPN (Q2) of the designed SCR (1) and subsequently reroutes the current path through the Q1 of the SCR (2) providing effective ESD protection for any medium voltage output driver exposed to ESD events up to 2KV HBM.

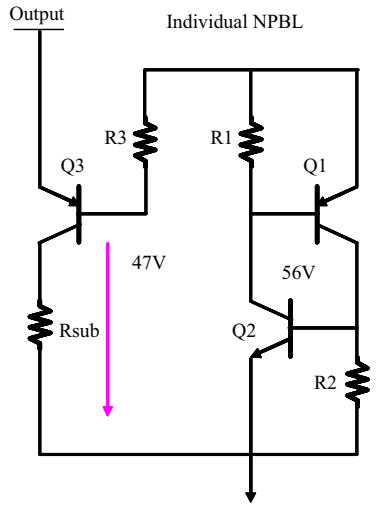

Fig. 8 Schematic view of a conventional ESD protection output driver

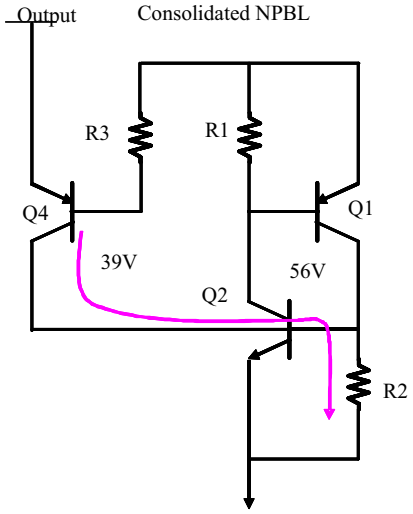

Fig. 9 Schematic view of the consolidated NPBL that allows self-triggered SCR

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